

WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:
programmable logic circuitry;
embedded processor circuitry comprising a processor; and
shared I/O circuitry coupled to the embedded processor circuitry and the
programmable logic circuitry that comprises a plurality of I/O pins which are accessible by
the processor and the programmable logic circuitry.
2. The integrated circuit of claim 1 wherein the shared I/O circuitry
further comprises a plurality of output driver circuits, each coupled to one of the I/O pins, that
drive signals sent to the I/O pins.
3. The integrated circuit of claim 1 wherein the shared I/O circuitry
further comprises a plurality of input driver circuits, each coupled to one of the I/O pins, that
drive signals received on the I/O pins.
4. The integrated circuit of claim 1 wherein the shared I/O circuitry
further comprises:
a first multiplexer coupled to receive a first data signal from the programmable
logic circuitry at a first input and a second data signal from the embedded processor circuitry
at a second input; and
a driver circuit that drives ^{an} the output of the first multiplexer onto a first one of
the I/O pins.
5. The integrated circuit of claim 4 wherein the first multiplexer selects
the first data signal or the second data signal in response to a control signal stored in a
register, and wherein the processor can write to the register to gain access to the first I/O pin.
6. The integrated circuit of claim 4 wherein the shared I/O circuitry
further comprises JTAG circuitry coupled between the first multiplexer and the driver circuit.
7. The integrated circuit of claim 4 wherein the shared I/O circuitry
further comprises:
a second multiplexer coupled to receive an output enable signal from the
programmable logic circuitry at a first input and an output enable signal from the embedded

5 processor circuitry at a second input, wherein the output of the second multiplexer drives a
6 tri-state input of the driver circuit.

1 8. The integrated circuit of claim 7 wherein JTAG is circuitry coupled
2 between the second multiplexer and the tri-state input of the driver circuit.

1 9. The integrated circuit of claim 1 wherein the shared I/O circuitry
2 further comprises a plurality of switches that couple signals received at the I/O pins to data
3 input signal lines to the embedded processor circuitry.

1 10. The integrated circuit of claim 9 wherein the shared I/O circuitry
2 further comprises a plurality of driver circuits coupled to the I/O pins that drive signals
3 received on the I/O pins to the programmable logic circuitry and the embedded processor
4 circuitry.

1 11. The integrated circuit of claim 10 wherein the shared I/O circuitry
2 further comprises JTAG circuitry coupled between the driver circuits and the switches.

1 obj 12. The integrated circuit of claim 1 wherein the programmable logic
2 circuitry comprises snoop circuitry that monitors input signals received at the I/O pins and
3 transmitted to the embedded processor circuitry.

1 obj 13. The integrated circuit of claim 12 wherein the snoop circuitry performs
2 debugging functions on the input signals received at the I/O pins and transmitted to the
3 embedded processor circuitry.

1 14. The integrated circuit of claim 1 wherein the shared I/O circuitry
2 further comprises a plurality of multiplexers which select from a first plurality of control
3 signals from the programmable logic circuitry and a second plurality of control signals from
4 the embedded processor circuitry to provide a third plurality of control signals which
5 determine an I/O standard for the shared I/O circuitry.

1 15. The integrated circuit of claim 1 wherein data bits are loaded into the
2 programmable logic circuitry through the I/O pins of the shared I/O circuitry to configure the
3 programmable logic circuitry.

1 16. The integrated circuit of claim 1 wherein the integrated circuit further
2 comprises a power up mode during which the I/O pins in the shared I/O circuitry are
3 accessible by the programmable logic circuitry by default.

1 17. The integrated circuit of claim 1 wherein the shared I/O circuitry loads
2 data bits into the programmable logic circuitry and the processor during a Boot from Flash
3 Mode.

1 18. The integrated circuit of claim 1 wherein the shared I/O circuitry
2 alternately loads a stream of data bits received at the I/O pins into the processor and the
3 programmable logic circuitry.

1 19. An integrated circuit, comprising:
2 a programmable logic portion comprising a plurality of I/O pins;
3 a processor; and
4 shared I/O circuitry that provides circuitry in the programmable logic portion
5 and the processor with signal access to the I/O pins.

1 20. A method for transmitting data signals to and from an integrated
2 circuit, the method comprising:
3 transmitting a first input signal received at an I/O pin to programmable logic
4 circuitry on the integrated circuit;
5 transmitting a second input signal received at the I/O pin to a processor on the
6 integrated circuit;
7 transmitting a first output signal from the programmable logic circuitry to the
8 I/O pin; and
9 transmitting a second output signal from the processor to the I/O pin.

1 21. The method of claim 20 wherein transmitting the second input signal
2 received at the I/O pin to the processor further comprises maintaining a switch ON.

1 22. The method of claim 20 wherein transmitting the first output signal
2 from the programmable logic circuitry to the I/O pin further comprises selecting the first
3 output signal using a first multiplexer and applying an output signal of the first multiplexer to
4 a driver circuit.

1 23. The method of claim 22 wherein transmitting the first output signal
2 from the programmable logic circuitry to the I/O pin further comprises selecting an output
3 enable signal from the programmable logic circuitry using a second multiplexer and applying
4 an output signal of the second multiplexer to a tri-state input of the driver circuit.

1 24. The method of claim 20 wherein transmitting the second output signal
2 from the processor to the I/O pin further comprises selecting the second output signal using a
3 first multiplexer and applying an output signal of the first multiplexer to a driver circuit.

1 25. The method of claim 24 wherein transmitting the second output signal
2 from the processor to the I/O pin further comprises selecting an output enable signal from the
3 processor using a second multiplexer and applying an output signal of the second multiplexer
4 to a tri-state input of the driver circuit.

1 26. The method of claim 20 further comprising selecting a first control
2 signal from the programmable logic circuitry or a second control signal from the processor to
3 set an I/O standard for the I/O pin.

1 27. The method of claim 20 wherein transmitting the first input signal
2 received at the I/O pin to the programmable logic circuitry further comprises monitoring
3 signals received at the I/O pin and transmitted to the processor.

1 28. A method for augmenting the functionality of an integrated circuit
2 comprising programmable logic circuitry, the method comprising:
3 adding a processor to the integrated circuit;
4 adding shared I/O pins to the integrated circuit; and
5 adding a first plurality of multiplexing circuits to the integrated circuit that
6 control access to the I/O pins by data signals from the programmable logic circuitry and the
7 processor.

1 29. The method of claim 28 further comprising:
2 adding a second plurality of multiplexing circuits that select signals from the
3 processor and the programmable logic circuitry which determine an I/O standard for the
4 shared I/O pins.

1 30. The method of claim 28 further comprising:

2 adding output drivers to each of the shared I/O pins which drive the data
3 signals from the programmable logic circuitry and the processor to the shared I/O pins; and
4 adding input drivers to each of the shared I/O pins which drive signals
5 received at the I/O pins to the programmable logic circuitry and the processor to the shared
6 I/O pins.

1 31. The method of claim 28 further comprising:
2 selecting a first data signal from the programmable logic circuitry or a second
3 data signal from the processor to be transmitted to a first one of the shared I/O pins using one
4 of the multiplexing circuits which is controlled by a control signal stored in a register,
5 wherein the processor can write to the register to gain access to the first shared I/O pin.

1 32. The method of claim 28 wherein the first plurality of multiplexing
2 circuits select enable signals from the programmable logic circuitry or the processor, the
3 enable signals determining whether the programmable logic circuitry or the processor
4 accesses the shared I/O pins.

1 33. An integrated circuit, comprising:
2 a programmable logic portion;
3 an embedded logic portion adjacent to a first edge of the integrated circuit, the
4 embedded logic portion comprising a processor; and
5 a shared I/O portion in between the programmable logic portion and the
6 embedded logic portion, the shared I/O portion comprising first I/O pins that are accessible
7 by circuitry in the programmable logic portion and the embedded logic portion.

1 34. The integrated circuit of claim 33 further comprising a fourth portion
2 that includes second I/O pins adjacent to second, third, and fourth edges of the integrated
3 circuit.

1 35. The integrated circuit of claim 34 wherein the programmable logic
2 portion is surrounded by the shared I/O and the fourth portions of the integrated circuit.

1 36. The integrated circuit of claim 33 further comprising a fourth portion
2 of the integrated circuit adjacent to the shared I/O portion that comprises first multiplexers
3 which select data signals from the programmable logic portion and the embedded logic
4 portion to be driven onto the first I/O pins.

1 37. The integrated circuit of claim 36 wherein the fourth portion of the
2 integrated circuit further comprises second multiplexers which select I/O standard signals
3 from the programmable logic portion and the embedded logic portion.

1 /38. A method for operating an integrated circuit comprising a
2 programmable logic portion, a processor portion having a processor, and I/O pins that are
3 accessible by the programmable logic portion and the processor portion, the method
4 comprising:

5 transmitting input signals received at the I/O pins to the programmable logic
6 portion during power up of the integrated circuit; and

7 transmitting output signals from the programmable logic portion to the I/O
8 pins during the power up of the integrated circuit.

1 = 39. A method for operating an integrated circuit comprising a
2 programmable logic portion, a processor portion having a processor, and I/O pins that are
3 accessible by the programmable logic portion and the processor portion, the method
4 comprising:

5 accessing bits stored in a Flash interface external to the integrated circuit to
6 obtain boot code for the processor using the I/O pins; and

7 accessing bits stored in the Flash interface for the programmable logic portion
8 using the I/O pins.

1 /40. A method for operating an integrated circuit comprising a
2 programmable logic portion, a processor portion having a processor, and I/O pins that are
3 accessible by the programmable logic portion and the processor portion, the method
4 comprising:

5 transmitting data bits through some of the I/O pins to configure circuitry
6 within the programmable logic portion; and

7 transmitting data bits through some of the I/O pins to configure circuitry
8 within the processor.

1 41. A method for operating an integrated circuit comprising a
2 programmable logic portion, a processor portion having a processor, and I/O pins that are
3 accessible by the programmable logic portion and the processor portion, the method
4 comprising:

transmitting a first signal stream received at a first of the I/O pins to circuitry in the programmable logic portion; and

transmitting a second signal stream received at the first I/O pin to circuitry in the processor portion concurrently with the first signal stream.

42. The method of claim 41 wherein transmitting the second signal stream further comprises switching a switch ON and OFF in response to a control signal to dynamically toggle signals received at the first I/O pin between the circuitry in the programmable logic portion and the circuitry in the processor portion.